

Claims

1. An electronic assembly for switching electric power, comprising
 - two power supply buses spaced from each other, between which semiconductor switches to be driven by means of a control input are arranged at a power output for providing electric power,
 - a capacitor arrangement bridging the two power supply buses, which extends at least partially over the length of the power supply buses,
 - two contact layers originating from one each of the power supply buses and covering the capacitor arrangement at least partially, with the contact layers comprising free end portions which mutually project one another towards the respective other one of the power supply buses, and with
 - the two contact layers having a freely accessible contact area each which is adapted for contact making with correspondingly configured power terminals.
2. The electronic assembly according to Claim 1, with the two contact layers having a common covering zone in which they are separated from one another by an insulation.
3. The electronic assembly according to Claim 1 or 2, with the two contact layers having contact areas each which are spaced from one another essentially in the direction of the longitudinal extension of the power supply buses.
4. The electronic assembly according to one of Claims 1 to 3, with the two power supply buses being arranged essentially parallel to one another.
5. The electronic assembly according to one of Claims 1 to 4, with the semiconductor switches which are arranged between the two power supply buses being arranged on a substrate which is preferably adapted for contact making with a cooling device.
6. The electronic assembly according to one of Claims 1 to 5, with the power output comprising a busbar which is arranged between the two power supply buses.
7. The electronic assembly according to one of Claims 1 to 6, with
 - the semiconductor switches being formed by high-speed switching low-loss field effect transistors (FETs) or by high-speed switching low-loss bipolar transistors with insulated gate terminals (IGBTs) with, in particular, MOSFETs with integrated free-wheeling diodes

or with additional external free-wheeling diodes which are connected in parallel with the transistors being employed.

8. The electronic assembly according to one of Claims 1 to 7, with

- plane contact sheets which are angled for a height compensation or a lateral compensation being soldered or welded as electrical connection between the printed conductors arranged on the circuit board or the substrate, or the power supply buses or the busbar, respectively, on the one hand, and contact making points of the semiconductors, on the other hand.

9. The electronic assembly according to Claim 8, with

- the semiconductors having large plane contact making points with a coating of noble metal.

10. The electronic assembly according to one of Claims 1 to 7, with

- at least two semiconductor switches (14, 22; 24, 18, 26) which are connected in series under the formation of a half-bridge (12a, 12c, 12c);

- each of the semiconductor switches (14, 22; 24, 18, 26) having a control input (G) for the connection with a driving means;

- the first semiconductor switch (14, 16, 18) to be connected with its source terminal (S) to a high voltage potential (V_{SS});

- the second semiconductor switch (22, 24, 26) to be connected with its drain terminal (D) to a low voltage potential (V_{DD});

- for forming an output (A), the drain terminal (D) of each first semiconductor switch (14, 16, 18) being connected with the source terminal (S) of the respective second semiconductor switch (22, 24, 26); and

- at least one capacitor arrangement (52) being arranged between the high and the low voltage potential (V_{SS} , V_{DD});

- respective first semiconductor switches (14, 16, 18) being arranged with their source terminal (S) on a common first metallic conductor rail (60) to be connected with the high voltage potential (V_{SS});

- respective second semiconductor switches (22, 24, 26) being arranged with their source terminal (S) on a common second metallic conductor rail (62) which forms the output (A), with the second conductor rail (62) being arranged spaced from and adjacent to the first conductor rail (60);

- each second semiconductor switch (22, 24, 26) being connected with its drain terminal (D) to a common third metallic conductor rail (66) which is to be connected with the low

voltage potential (V_{DD}) being arranged spaced from and adjacent to the first and second conductor rail (60, 62);

- the capacitor arrangement (52) comprising a back-up capacitor (52a, ..., 52d) which is connected with the first and the third conductor rail (60, 66) via terminals, which encompasses the first and the second semiconductor switches (14, 22; 24, 18, 26; 20, 28) in such a manner that the semiconductor switches are located spatially between the corresponding conductor rails (60, 66) and the back-up capacitor (52a, ..., 52d);

- the control input (G) comprising a terminal (76) for the connection with the driving means in the area of a first face (78) of the conductor rails (60, 62, 68), and

- the output (A) comprising a terminal for the connection with an electric load in the area of a second face (82) of the second conductor rail (62), which is located opposite the first face.

11. The electronic assembly according to one of Claims 1 to 10, with

- the three rails (60, 62, 66) being mechanically firmly connected with each other by an electrically insulating circuit board (90).

12. The electronic assembly according to one of Claims 1 to 10, with

- the three rails (60, 62, 66) being mechanically firmly connected with each other by electrically insulating lands which are arranged between the individual conductor rails.

13. A power output stage of a driving means for a multiphase electrical machine, characterised in that at least one electronic assembly according to one of the previous claims is provided for each phase of the electrical machine, with the electronic assembly being arranged at least along a portion of the circumference of the electrical machine.